# POWER AMPLIFIER CIRCUIT


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## Abstract


PURPOSE:To decrease the reduction of efficiency at a low output voltage by connecting a gate voltage or base voltage control circuit to an input terminal of a power amplifier.

CONSTITUTION:An input signal from a signal input terminal 6 is inputted to a gate of a power amplifier circuit using an FET via an input power control circuit 2. An output of the amplifier circuit 1 is detected by an output power detection circuit 4 and outputted from an output terminal 8. Further, a drain of the FET is connected to a drain voltage control circuit 14. The input power control circuit 2 changes the input signal based on the signal from a power reduction signal input terminal 13 and a signal from the output voltage detection circuit 4. The signal from the terminal 13 is inputted also to a gate voltage control circuit 3 connected to the input terminal of the amplifier 1 and changes the gate voltage of the FET at power reduction. Thus, the reduction in the efficiency at a low output power is suppressed.